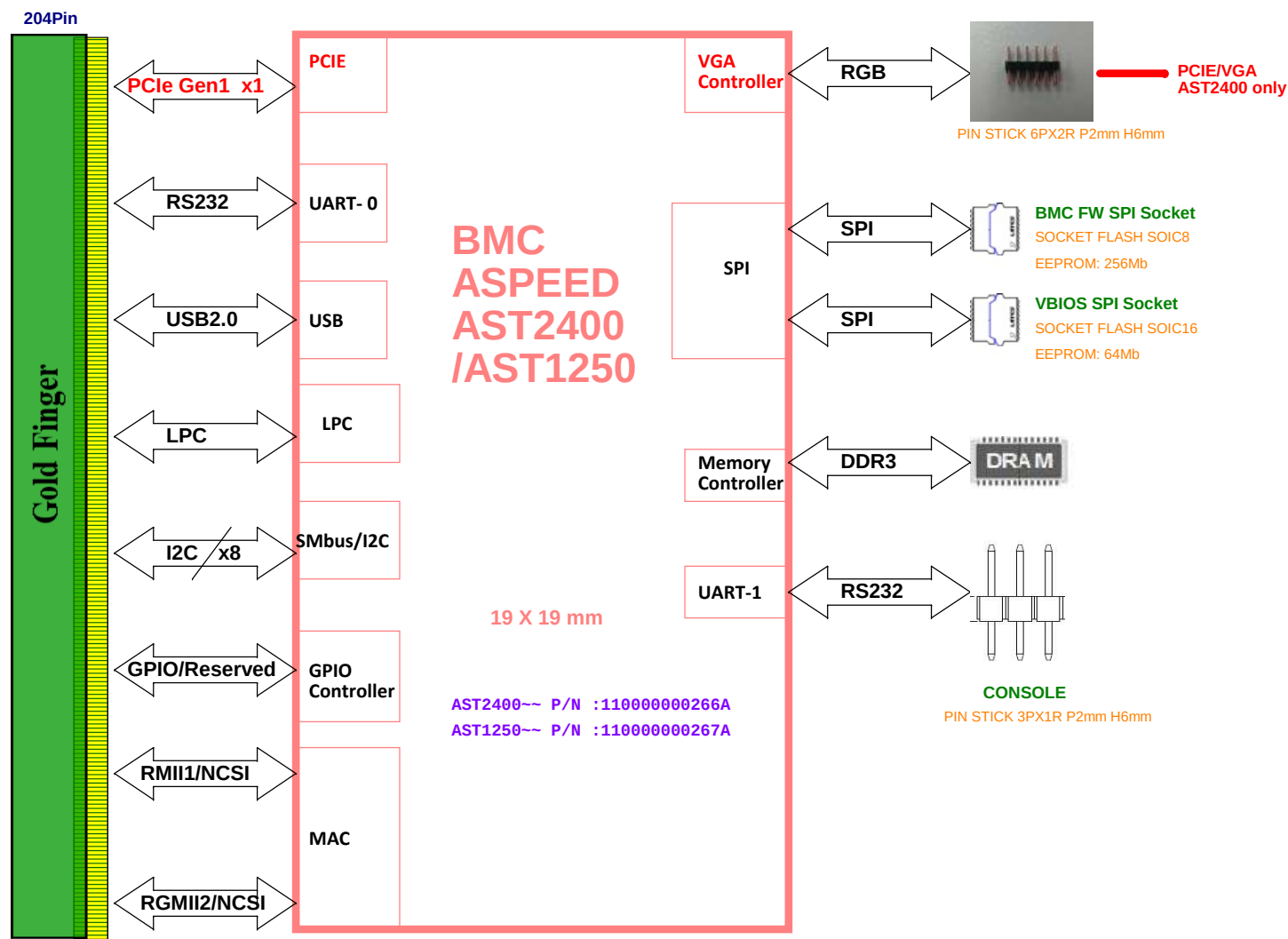




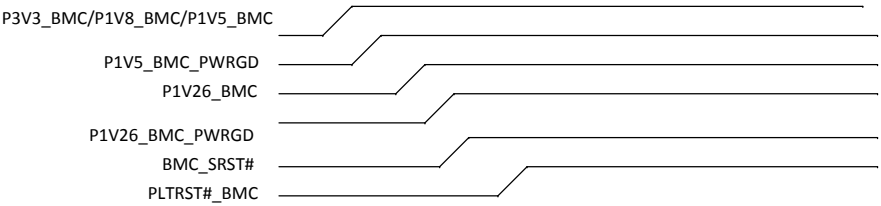
This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.



**Accton**  
Making Partnership Work

|                  |                      |               |
|------------------|----------------------|---------------|
| Model Name       |                      | Rev           |
| BDX-DE BMC Board |                      | R0A           |
| Size B           | Page Name            | Engineer      |
|                  | System Block Diagram | Jesse_Li      |
| Date:            | Friday, May 04, 2018 | Sheet 1 of 12 |

# BMC Power Squence



## Power Up Sequence

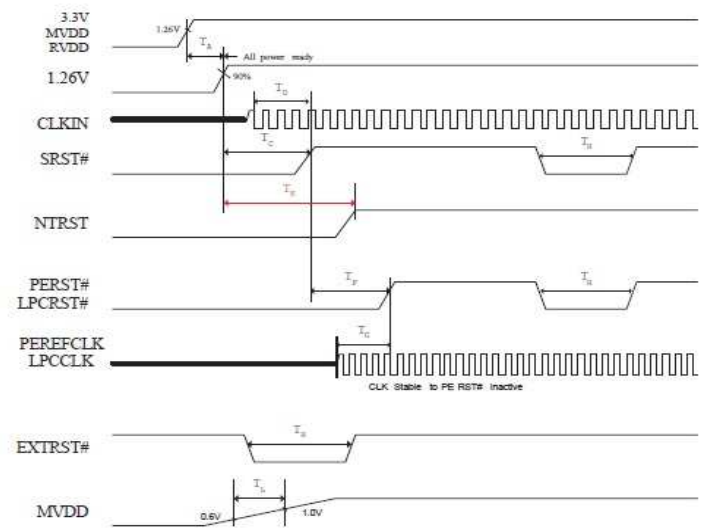


Figure 18: Power-up sequence

## Power-up Sequence Parameters

| PARAMETER                                                                   | SYMBOL | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------------------------|--------|-----|-----|-----|------|
| 3.3V/MVDD/RVDD to 1.26V delay                                               | $T_A$  | 0   |     |     | ms   |
| Power stable to power-on reset inactive                                     | $T_C$  | 1   |     |     | ms   |
| Power-on reset input rise time                                              |        | 0   |     | 100 | us   |
| CLKIN reference clock stable to power-on reset inactive                     | $T_D$  | 500 |     |     | us   |
| Power-on Reset to PCI-E/LPC reset, wait ID initialize by SOC (AST2400 only) | $T_F$  | 100 |     |     | ms   |
| PCI-E/LPC clock stable to reset inactive                                    | $T_G$  | 1   |     |     | ms   |
| Minimum valid reset pulse width                                             | $T_H$  | 1   |     |     | us   |
| Power stable to JTAG nTRST inactive delay                                   | $T_K$  | 10  |     |     | us   |
| DDR2/DDR3 MVDD power-up rise time 0.6V – 1.0V                               | $T_L$  | 800 |     |     | us   |

This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.



**Accton**  
Making Partnership Work

|                  |                      |          |         |
|------------------|----------------------|----------|---------|
| Model Name       |                      | Rev      |         |
| BDX-DE BMC Board |                      | R0A      |         |
| Size B           | Page Name            | Engineer |         |
|                  | BMC Power sequence   | Jesse_Li |         |
| Date:            | Friday, May 04, 2018 | Sheet    | 2 of 12 |

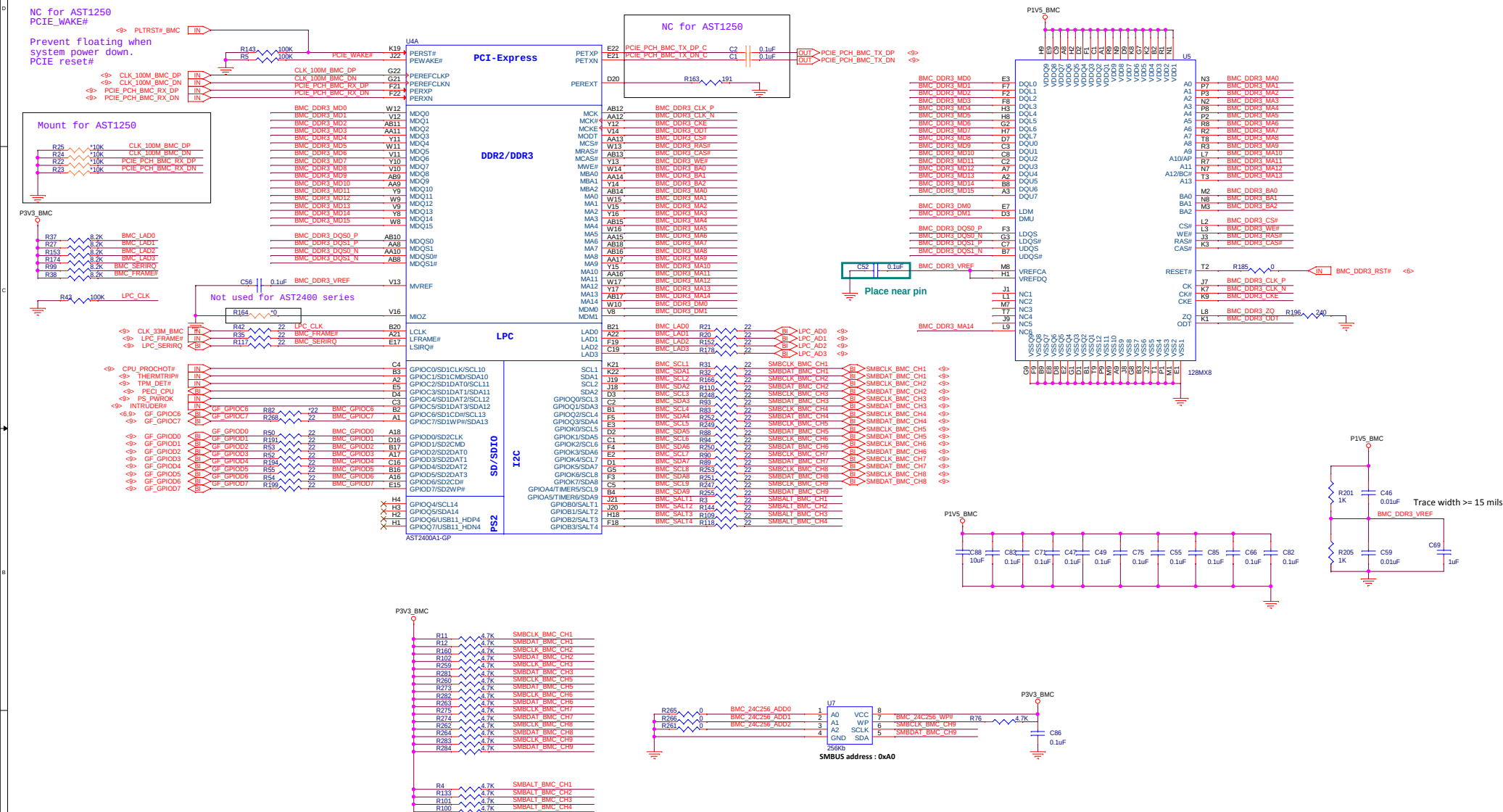
# BMC GPIO Table

This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.



**Accton**  
Making Partnership Work

|            |                |                      |          |       |         |
|------------|----------------|----------------------|----------|-------|---------|
| Model Name |                | BDX-DE BMC Board     |          | Rev   | R0A     |
| Size       | Page Name      |                      | Engineer |       |         |
| A          | BMC GPIO table |                      | Jesse_Li |       |         |
| Date:      |                | Friday, May 04, 2018 |          | Sheet | 3 of 12 |



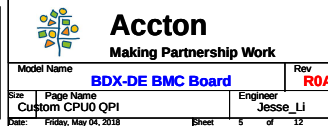
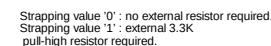
This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.

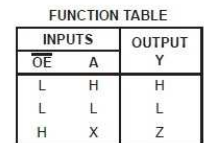


**Accton**

Making Partnership Work

|                  |                      |  |          |   |       |
|------------------|----------------------|--|----------|---|-------|
| Model Name       |                      |  | Rev      |   |       |
| BDX-DE BMC Board |                      |  | R0A      |   |       |
| Size             | Page Name            |  | Engineer |   |       |
| C                | CPU0 QPI             |  | Jesse_Li |   |       |
| Date:            | Friday, May 04, 2018 |  | Sheet    | 4 | of 12 |

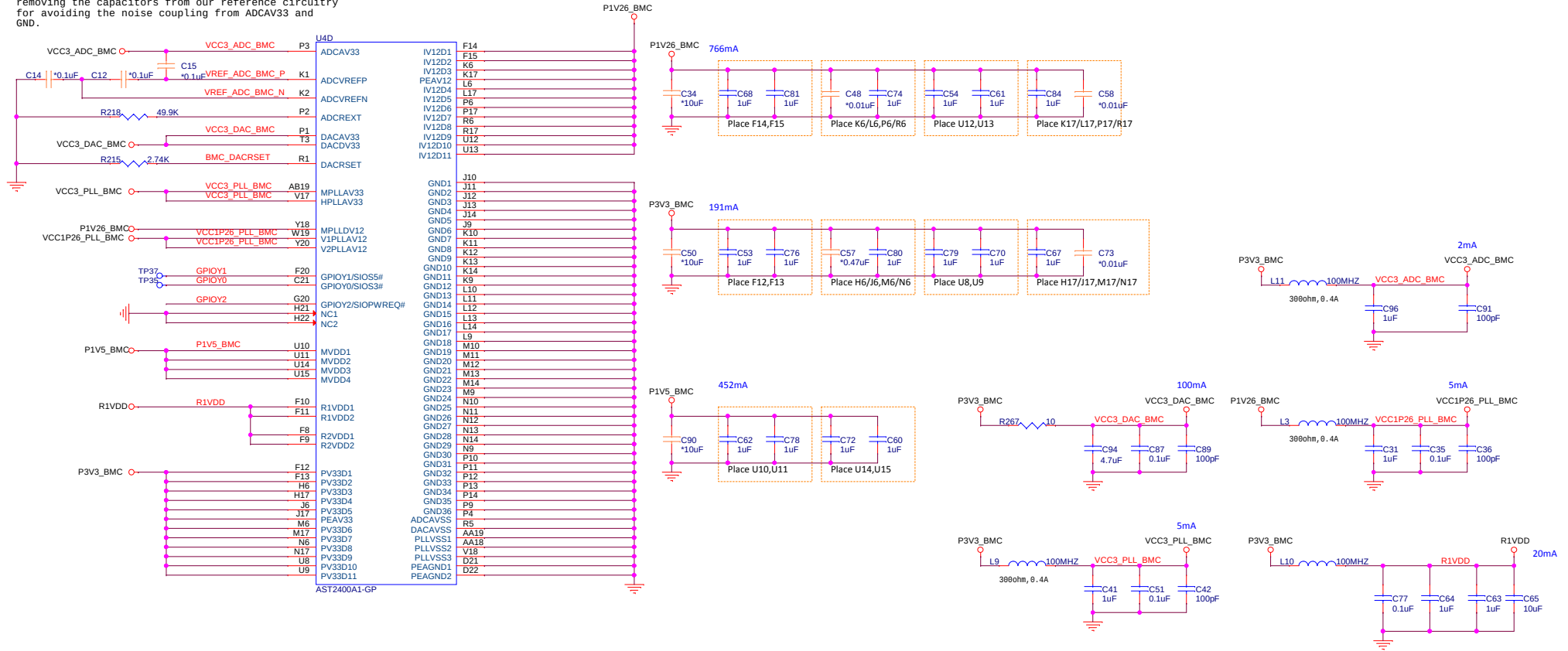




|                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                               |                                                                                                                                                        |                                                                                                                                    |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
|  <h1 style="margin: 0;">Accton</h1> <h2 style="margin: 0;">Making Partnership Work</h2>                                                                                                                                                                                                                                            |                                                                                                                                               |                                                                                                                                                        |                                                                                                                                    |
| <table border="1" style="width: 100%;"> <tr> <td style="width: 80%;"> <b>Model Name</b><br/> <div style="background-color: #007bff; color: white; padding: 5px; text-align: center; font-weight: bold;">BDX-DE BMC Board</div> </td> <td style="width: 20%;"> <b>Rev</b><br/> <div style="background-color: #dc3545; color: white; padding: 5px; text-align: center; font-weight: bold;">R0A</div> </td> </tr> </table> |                                                                                                                                               | <b>Model Name</b><br><div style="background-color: #007bff; color: white; padding: 5px; text-align: center; font-weight: bold;">BDX-DE BMC Board</div> | <b>Rev</b><br><div style="background-color: #dc3545; color: white; padding: 5px; text-align: center; font-weight: bold;">R0A</div> |
| <b>Model Name</b><br><div style="background-color: #007bff; color: white; padding: 5px; text-align: center; font-weight: bold;">BDX-DE BMC Board</div>                                                                                                                                                                                                                                                                  | <b>Rev</b><br><div style="background-color: #dc3545; color: white; padding: 5px; text-align: center; font-weight: bold;">R0A</div>            |                                                                                                                                                        |                                                                                                                                    |
| <b>Size</b><br><div style="background-color: #6c757d; color: white; padding: 5px; text-align: center; font-weight: bold;">C</div>                                                                                                                                                                                                                                                                                       | <b>Page Name</b><br><div style="background-color: #6c757d; color: white; padding: 5px; text-align: center; font-weight: bold;">CPU0 QPI</div> | <b>Engineer</b><br><div style="background-color: #6c757d; color: white; padding: 5px; text-align: center; font-weight: bold;">Jesse Li</div>           |                                                                                                                                    |
| <b>Date:</b> Friday, May 04, 2018                                                                                                                                                                                                                                                                                                                                                                                       | <b>Sheet</b> 6                                                                                                                                | <b>of</b> 12                                                                                                                                           |                                                                                                                                    |

Ref No. : A2400-02

The reference voltage of ADC (ADCVREFP and ADCVREFN) needs to be as clean as possible. We recommend removing the capacitors from our reference circuitry for avoiding the noise coupling from ADCAV33 and GND.



This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.

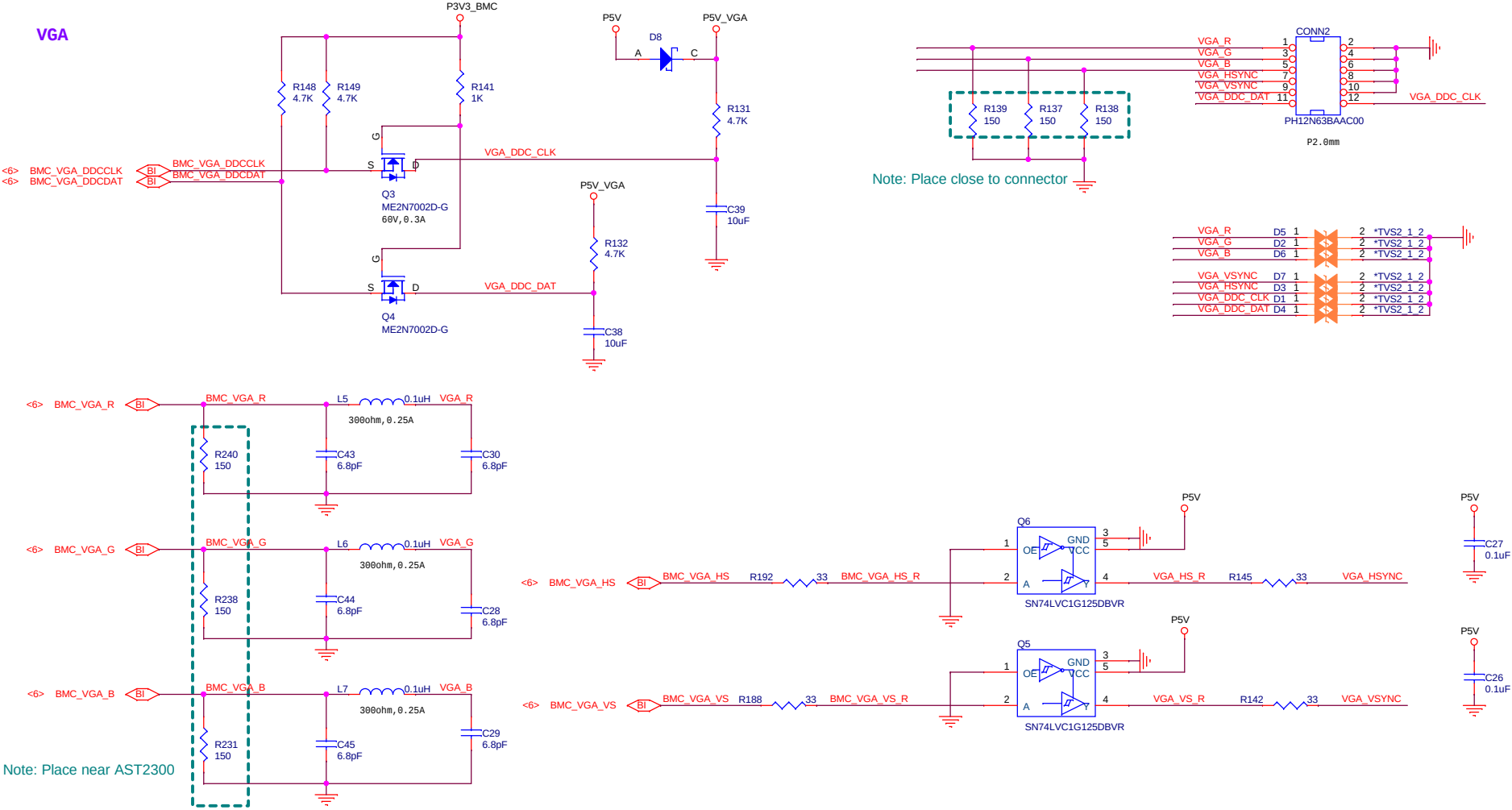


**Accton**

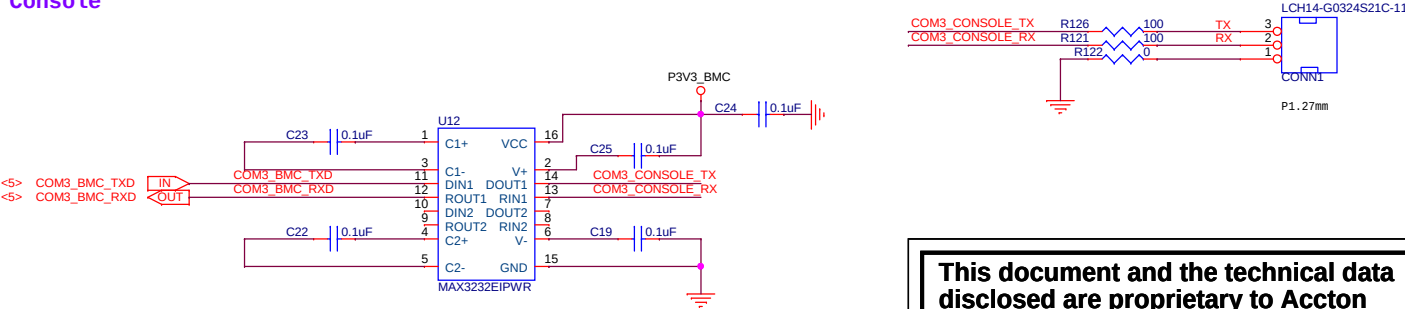
Making Partnership Worth

|                            |           |          |
|----------------------------|-----------|----------|
| Model Name                 |           | Rev      |
| BDX-DE BMC Board           |           | R0A      |
| Size                       | Page Name | Engineer |
| Custom CPU0 QPI            |           | Jesse_Li |
| Date: Friday, May 04, 2018 | Sheet     | 7 of 12  |

VGA



Console



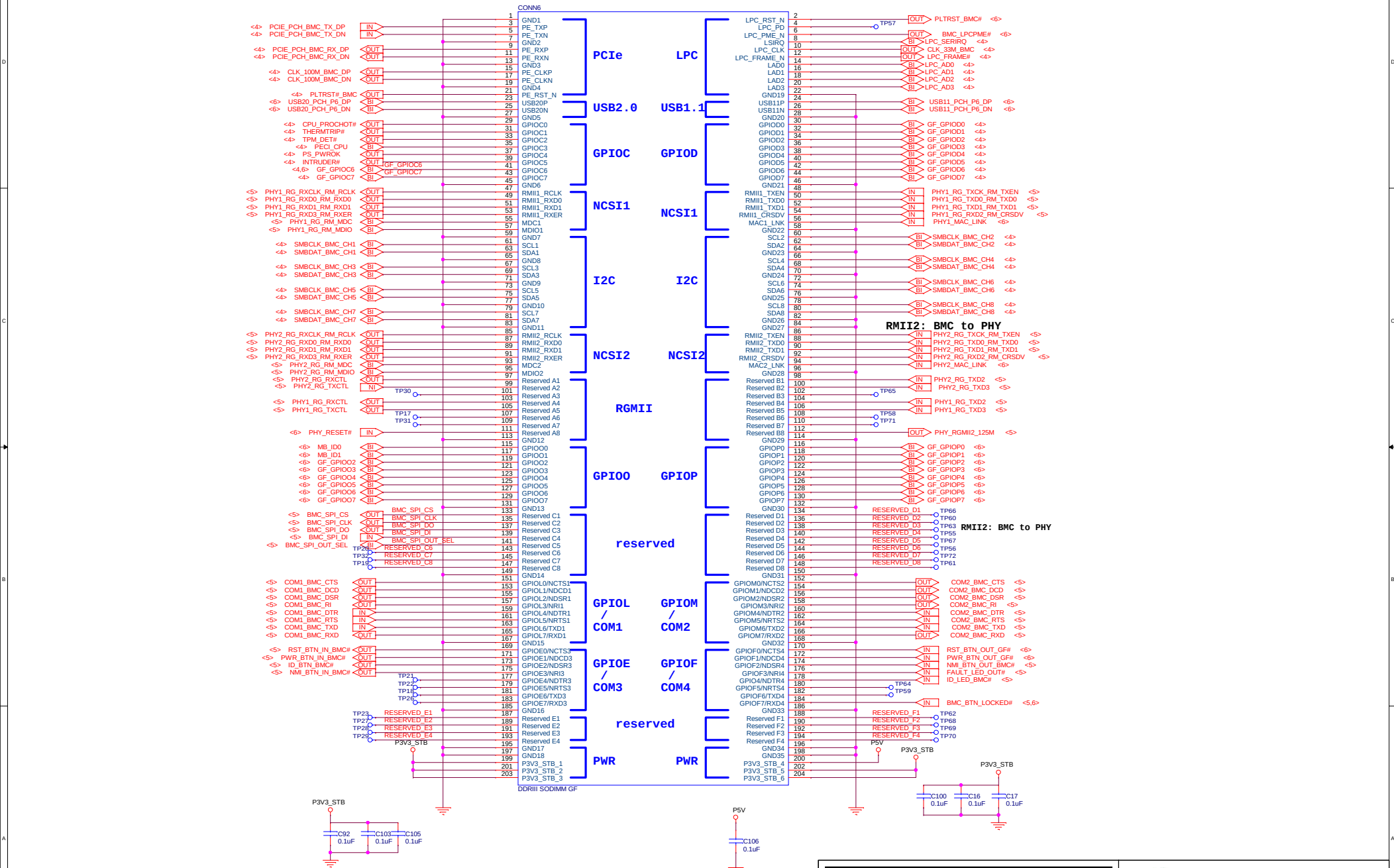
This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.



Accton

Making Partnership Work

|                  |                      |               |
|------------------|----------------------|---------------|
| Model Name       |                      | Rev           |
| BDX-DE BMC Board |                      | R0A           |
| Size             | Page Name            | Engineer      |
| Custom           | CPU0 QPI             | Jesse_Li      |
| Date:            | Friday, May 04, 2018 | Sheet 8 of 12 |



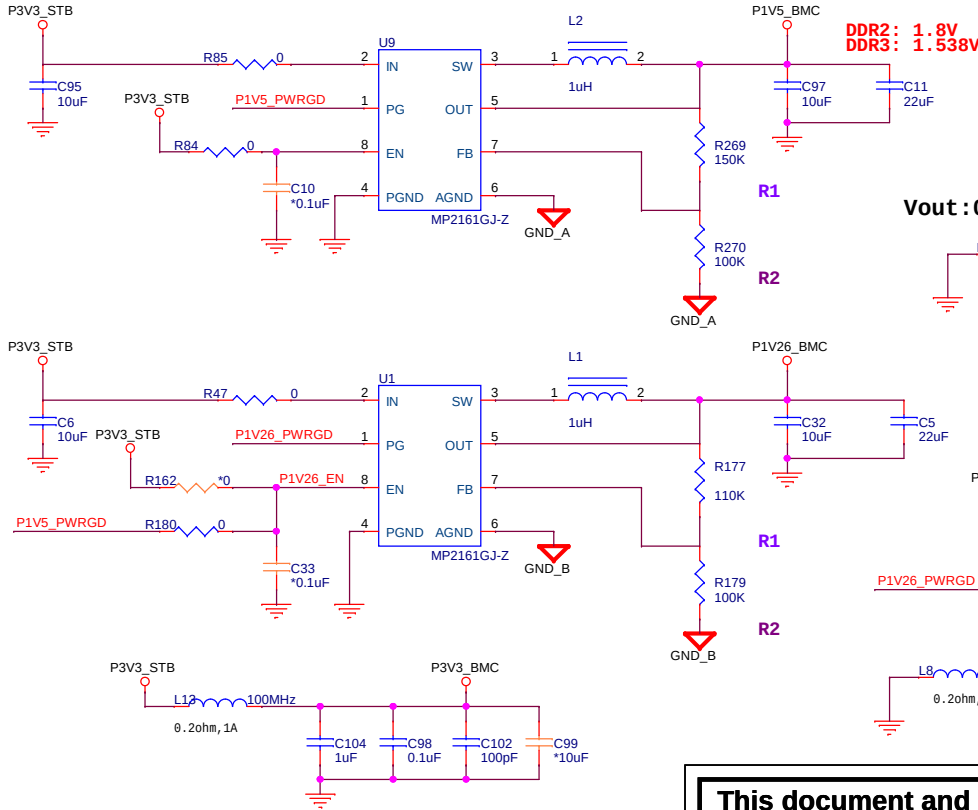
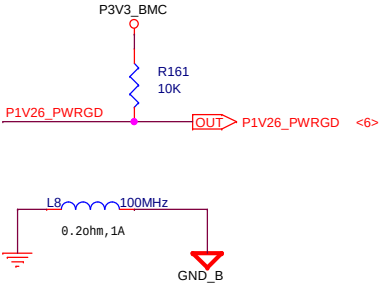
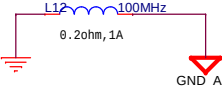


Table 1—Resistor Selection for Common Output Voltages

| V <sub>OUT</sub> (V) | R1 (kΩ) | R2 (kΩ)  |
|----------------------|---------|----------|
| 1.0                  | 200(1%) | 300(1%)  |
| 1.2                  | 200(1%) | 200(1%)  |
| 1.8                  | 200(1%) | 100(1%)  |
| 2.5                  | 200(1%) | 63.2(1%) |
| 3.3                  | 200(1%) | 44.2(1%) |

$V_{out} = 0.6(R1+R2) / R2$



This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.



**Accton**  
Making Partnership Work

|                            |                    |                   |
|----------------------------|--------------------|-------------------|
| Model Name                 |                    | Rev               |
| BDX-DE BMC Board           |                    | R0A               |
| Size B                     | Page Name CPU0 QPI | Engineer Jesse_Li |
| Date: Friday, May 04, 2018 |                    | Sheet 10 of 12    |

80 PORT

remove 80 port board

This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.



**Accton**  
Making Partnership Work

|                  |                        |                |
|------------------|------------------------|----------------|
| Model Name       |                        | Rev            |
| BDX-DE BMC Board |                        | R0A            |
| Size             | Page Name              | Engineer       |
|                  | Custom 80 PORT/BTN CTL | Jesse_Li       |
| Date:            | Friday, May 04, 2018   | Sheet 11 of 12 |

History

Project Name :SAU5081I-1014-ZZ

Version :R01  
PCB Part Number : 142000001219Ar0b

Modify Date: 2017/01/30

| Date       | Page | Description                        |
|------------|------|------------------------------------|
| 03/7/2016  | 4    | Change R163 to 191ohm              |
| 03/7/2016  | 4    | R76 insert 4.7K                    |
| 03/7/2016  | 5    | NI R15 3.3K                        |
| 03/7/2016  | 5    | R169 insert 3.3K                   |
| 03/7/2016  | 6    | Change R10 to 100ohm               |
| 03/10/2016 | 5    | NI R120                            |
| 03/10/2016 | 5    | U3 pin10 connect to GND            |
| 03/10/2016 | 5    | Change U2 to 512kb part            |
| 03/10/2016 | 4    | Add R283,R284                      |
| 03/10/2016 | 6    | Change R151 100K to GND            |
| 03/31/2016 | 5    | Add BMC_SPI_* 5 line               |
| 01/30/2017 | 6    | Add R97 for reset buffer pin 8 &10 |
| 01/30/2017 | 11   | remove 80 port board               |
|            |      |                                    |

This document and the technical data disclosed are proprietary to Accton Tech. Corp. and shall not be duplicated, used, released, or disclosed without expressed written permission.



**Accton**  
Making Partnership Work

|                            |                      |                      |
|----------------------------|----------------------|----------------------|
| Model Name                 |                      | Rev                  |
| BDX-DE BMC Board           |                      | R0A                  |
| Size<br>B                  | Page Name<br>History | Engineer<br>Jesse_Li |
| Date: Friday, May 04, 2018 | Sheet                | 12 of 12             |